Conventional Wafer Test Example

Figure 1A

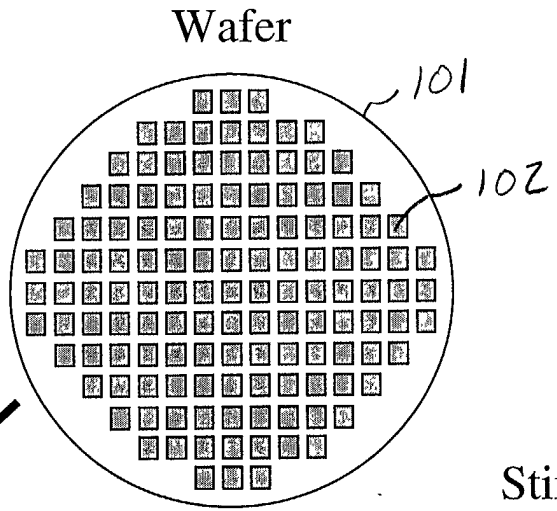


Figure 1B

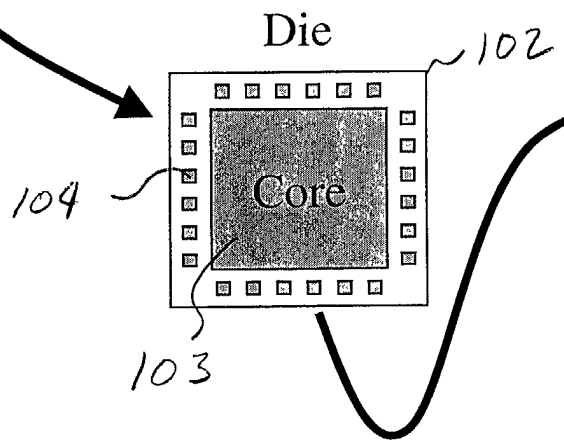
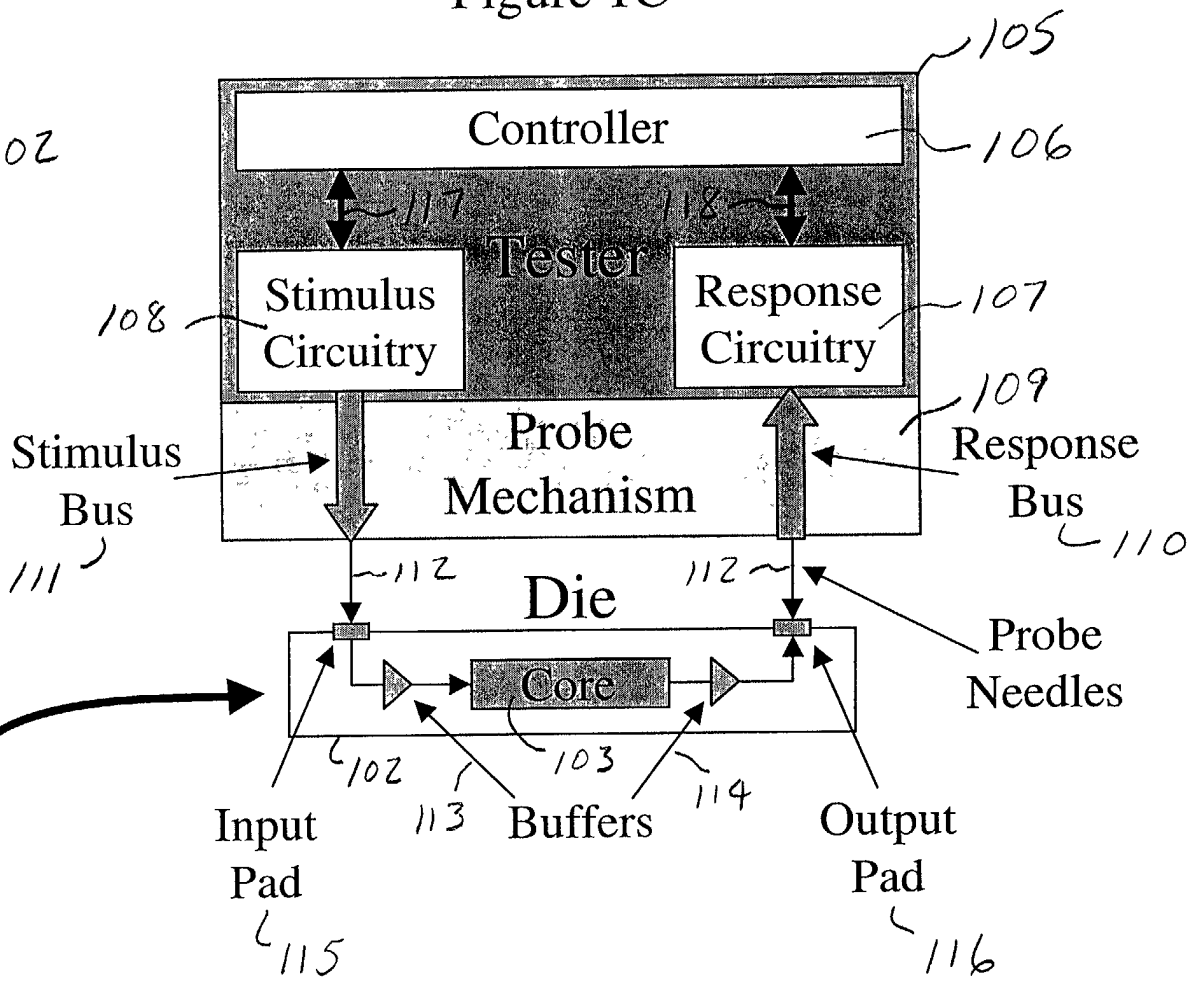
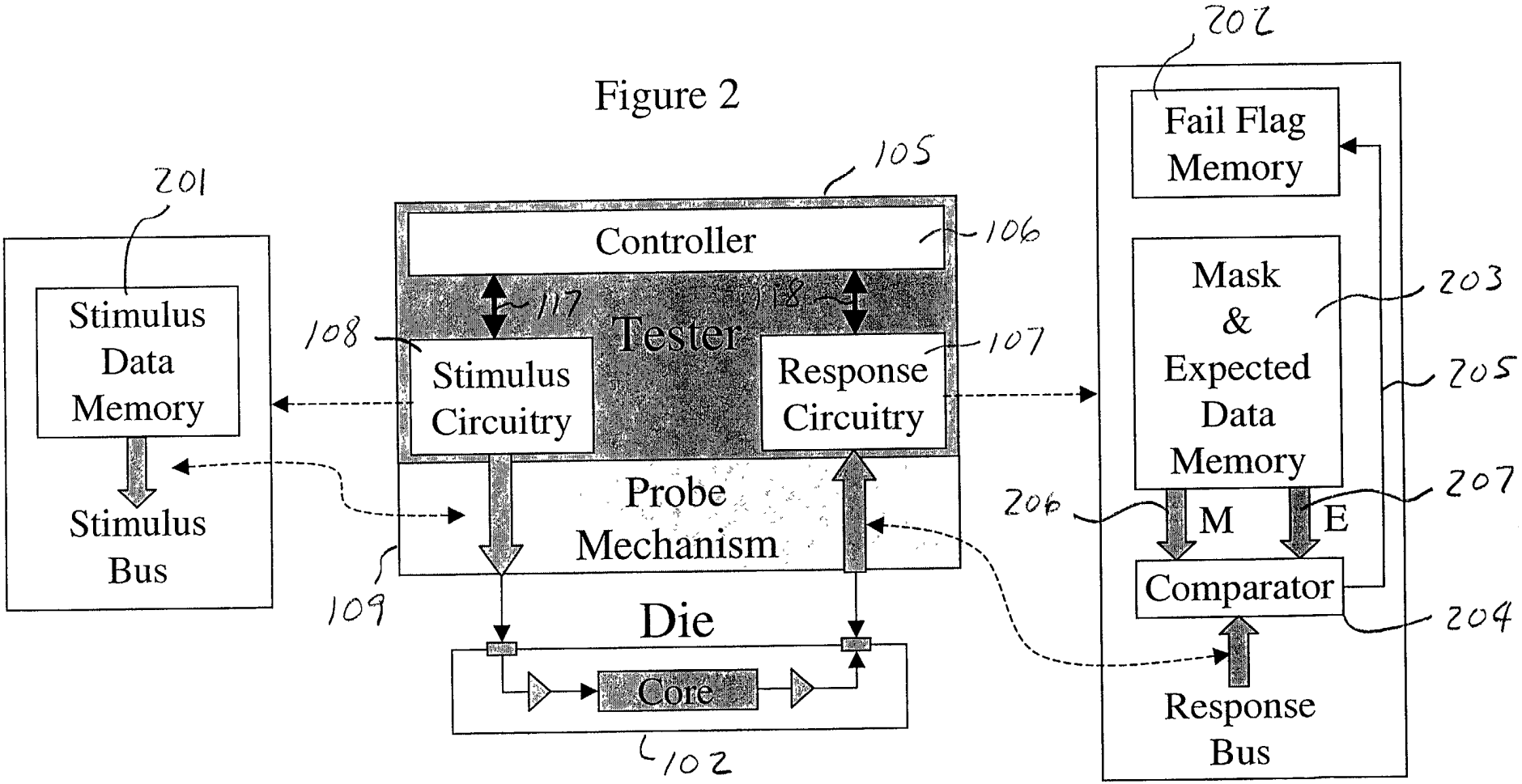


Figure 1C



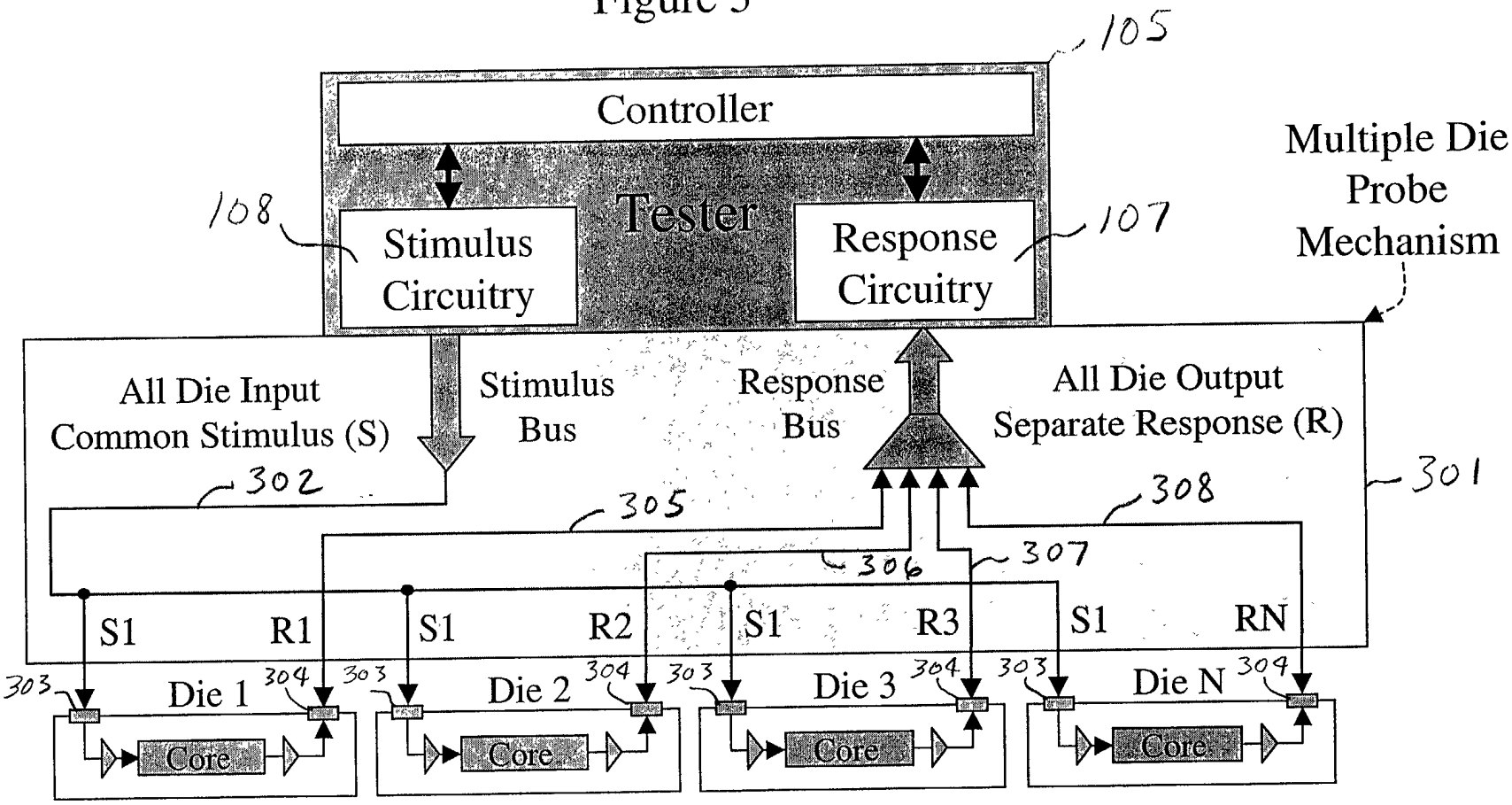
Conventional Tester
Stimulus & Response Circuitry

Figure 2



Multiple Die Probe Test Example

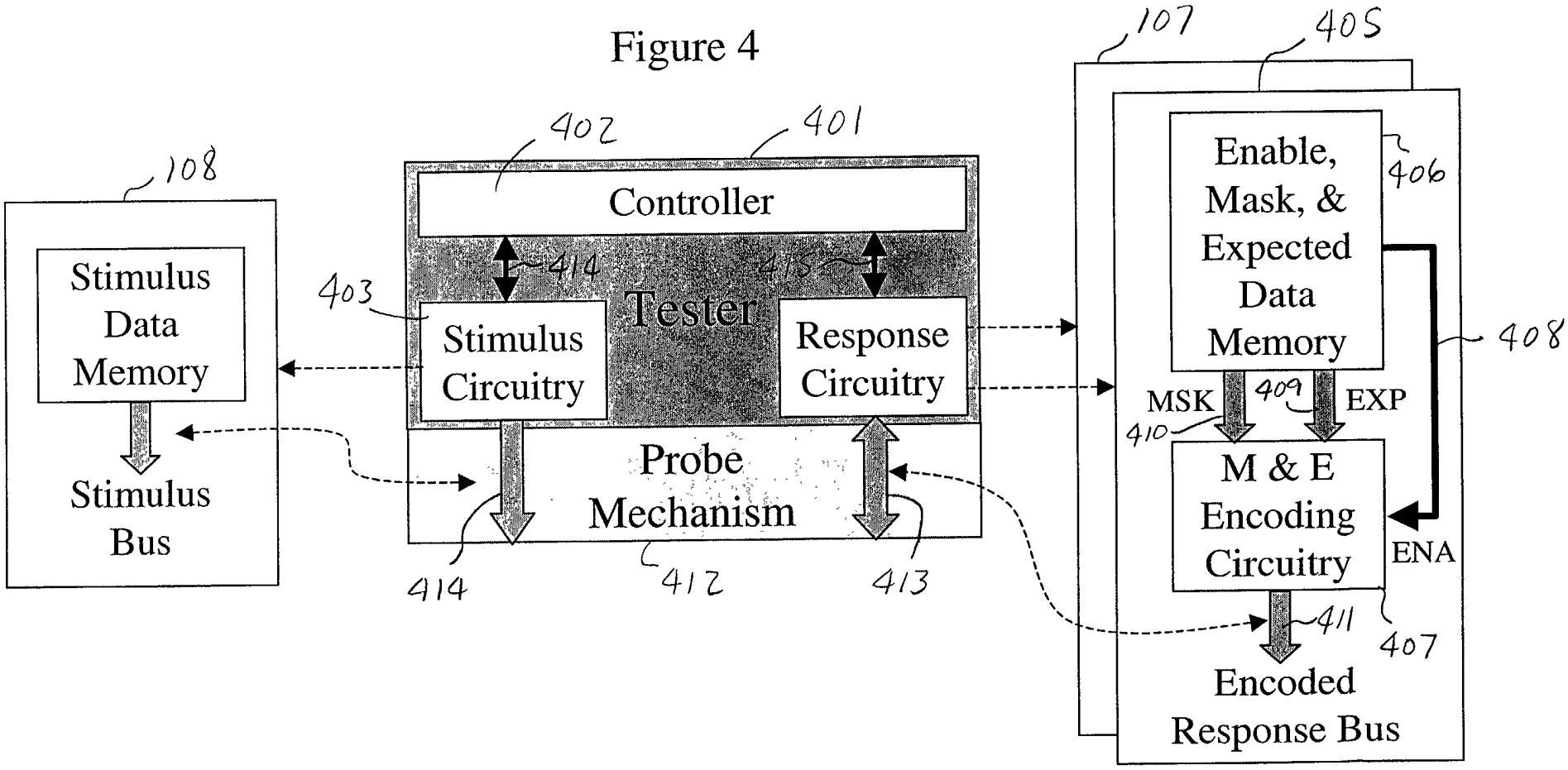
Figure 3



(Sum of R1-RN) <= (Tester Response Bus Width)

Adapting Testers
To Support Improved Wafer Testing

Figure 4



Mask & Expected Encoding Circuitry

Figure 5A

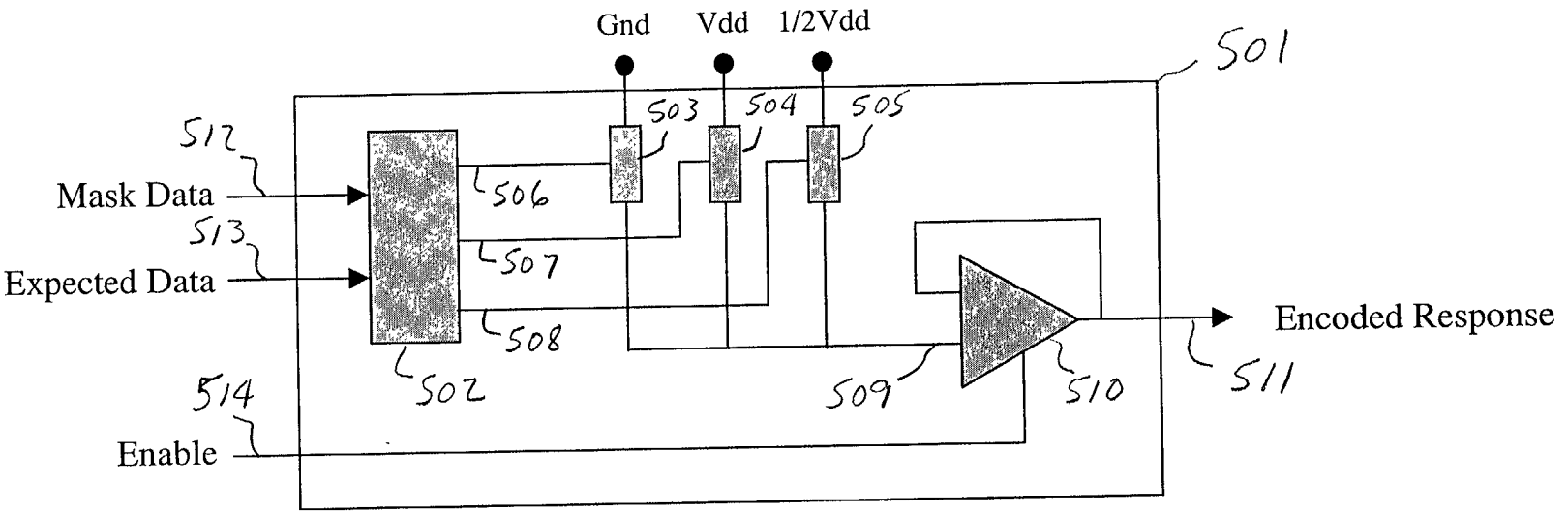


Figure 5B

ENA	MSK	EXP	ENR	Output Mode
0	0	0	Z	Disabled
1	0	0	Gnd	Low
1	0	1	Vdd	High
1	1	X	1/2Vdd	Mask

Adapting Die 2-State Outputs
To Support Improved Wafer Testing

Figure 6A

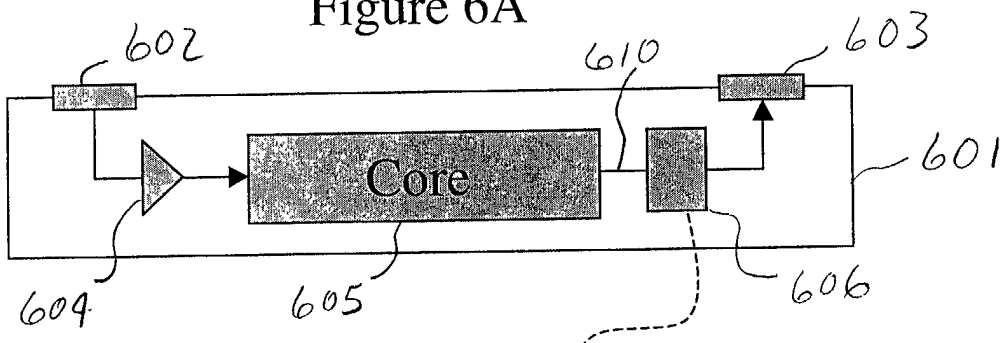
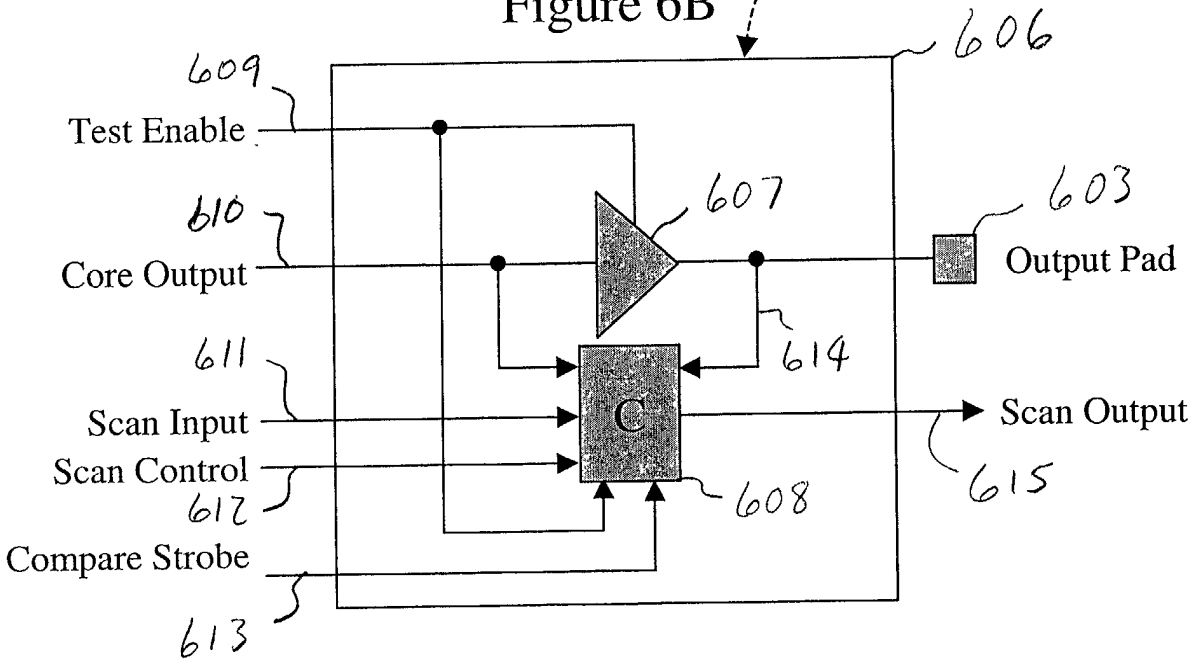


Figure 6B



Maskable Comparator For 2-State Outputs

Figure 7A

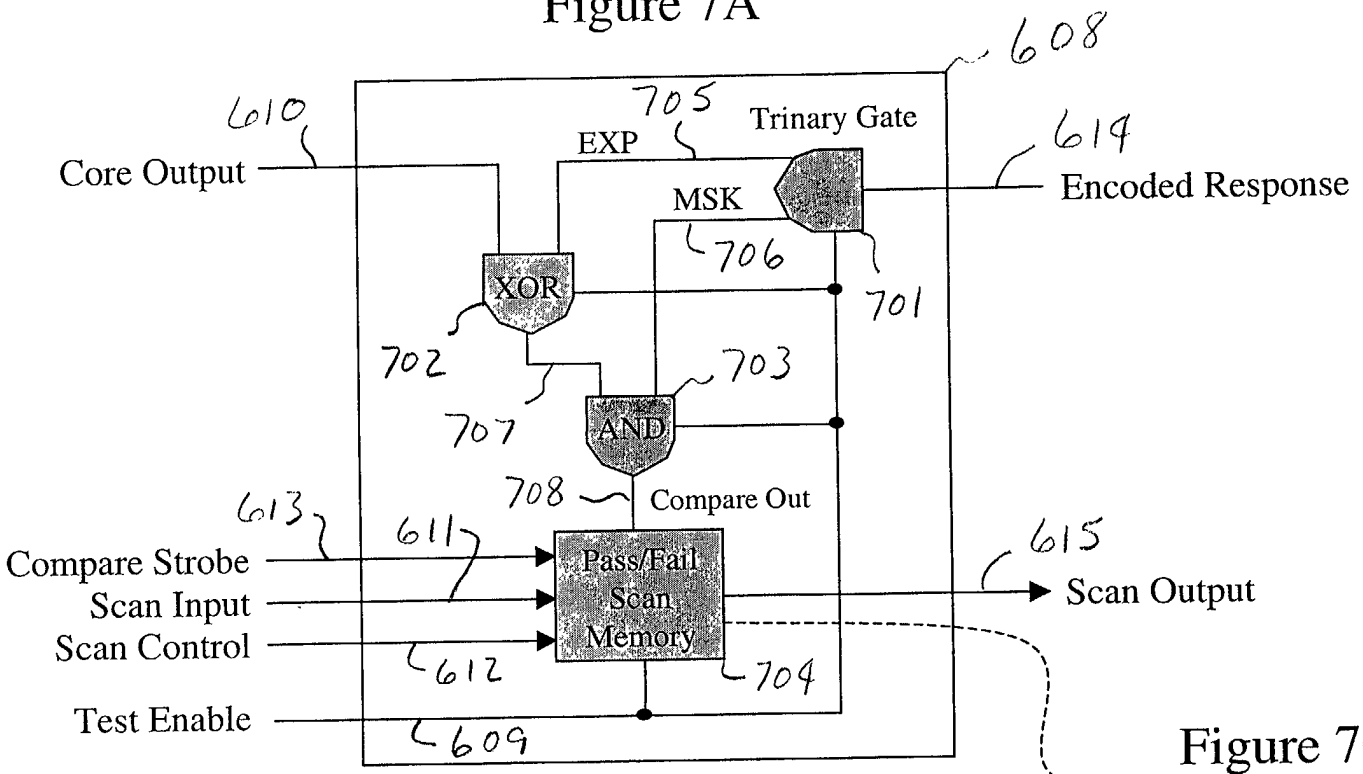
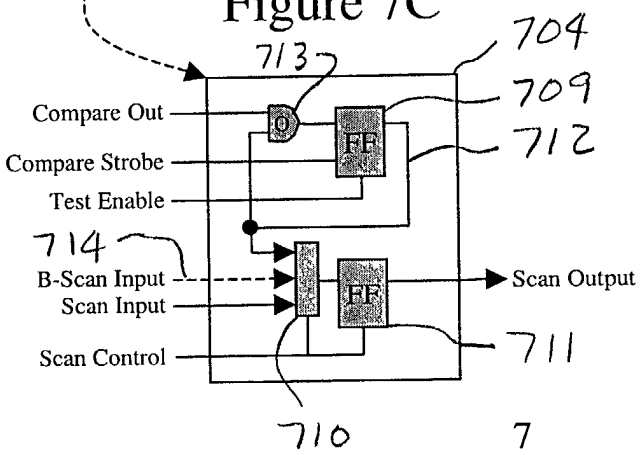


Figure 7B

TEN	ENR	MSK	EXP	Function Performed
0	X	X	X	Test Disabled
1	Gnd	1	0	Compare Low
1	Vdd	1	1	Compare High
1	1/2Vdd	0	X	Mask Compare

Figure 7C



Trinary Gate Circuit Example

Figure 8A

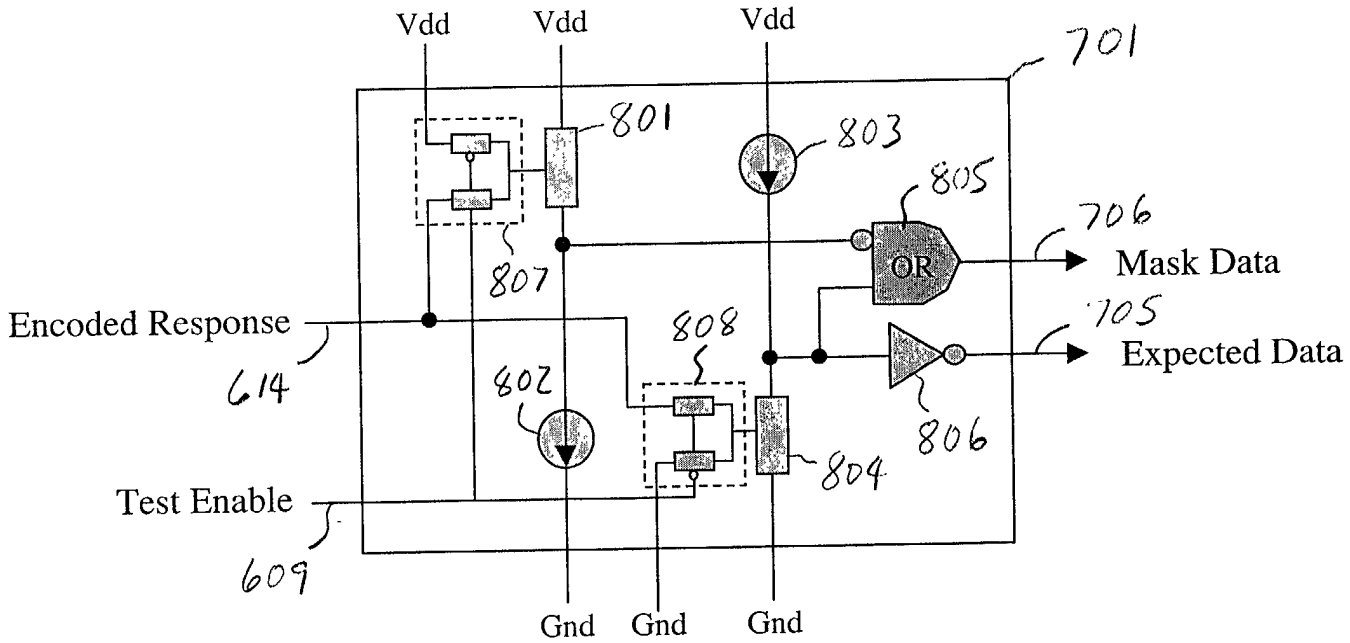


Figure 8B

TEN	ENR	MSK	EXP	Function Performed
0	X	1	0	Gate Disabled
1	Gnd	1	0	Output a Low
1	Vdd	1	1	Output a High
1	1/2Vdd	0	X	Output a Mask

Adapting Die 3-State Outputs
To Support Improved Wafer Testing

Figure 9A

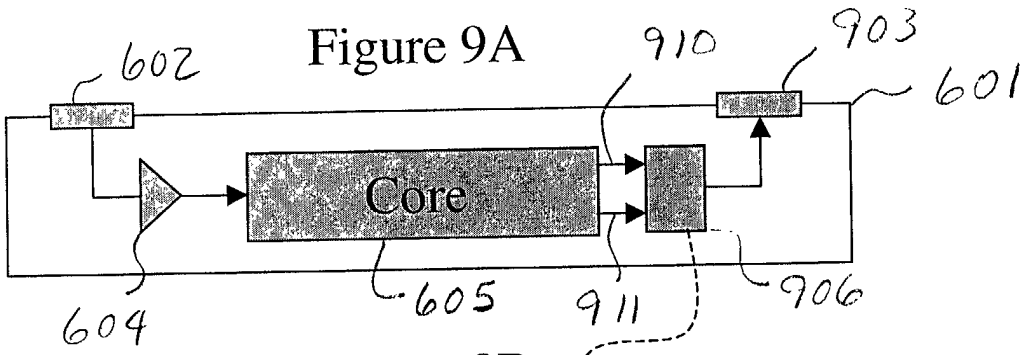
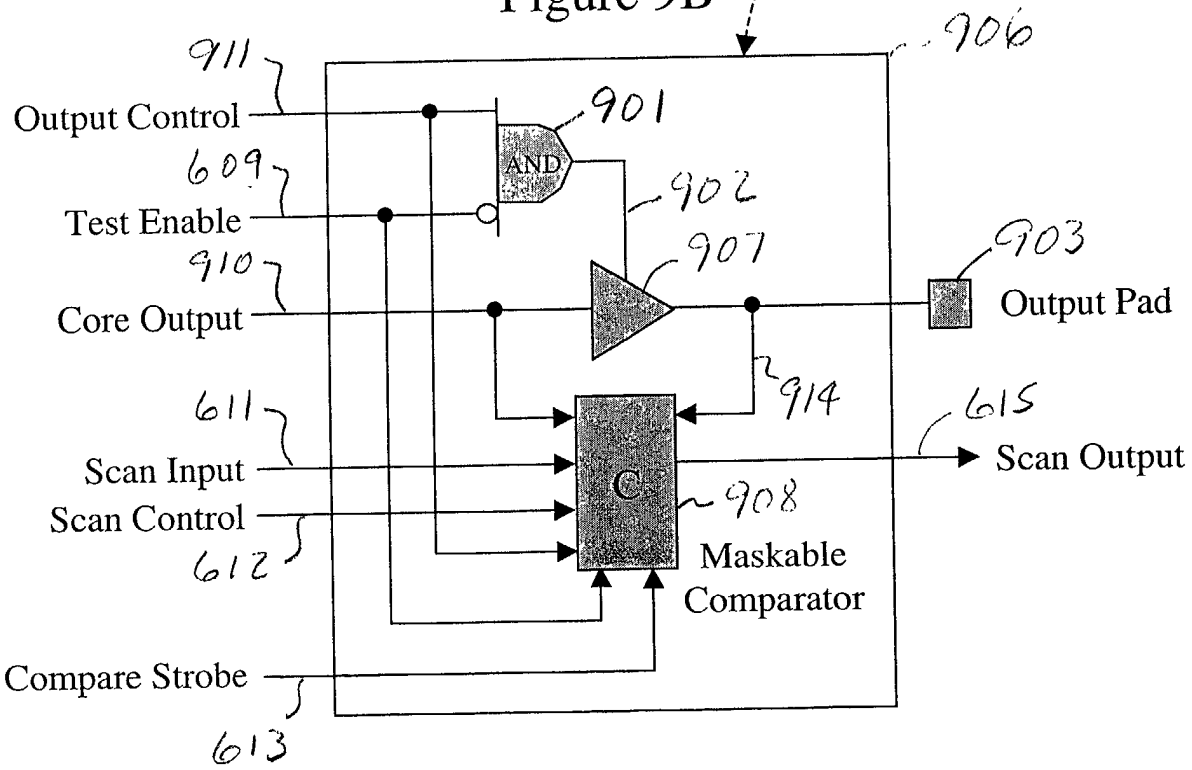


Figure 9B



Maskable Comparator For 3-State Outputs

Figure 10A

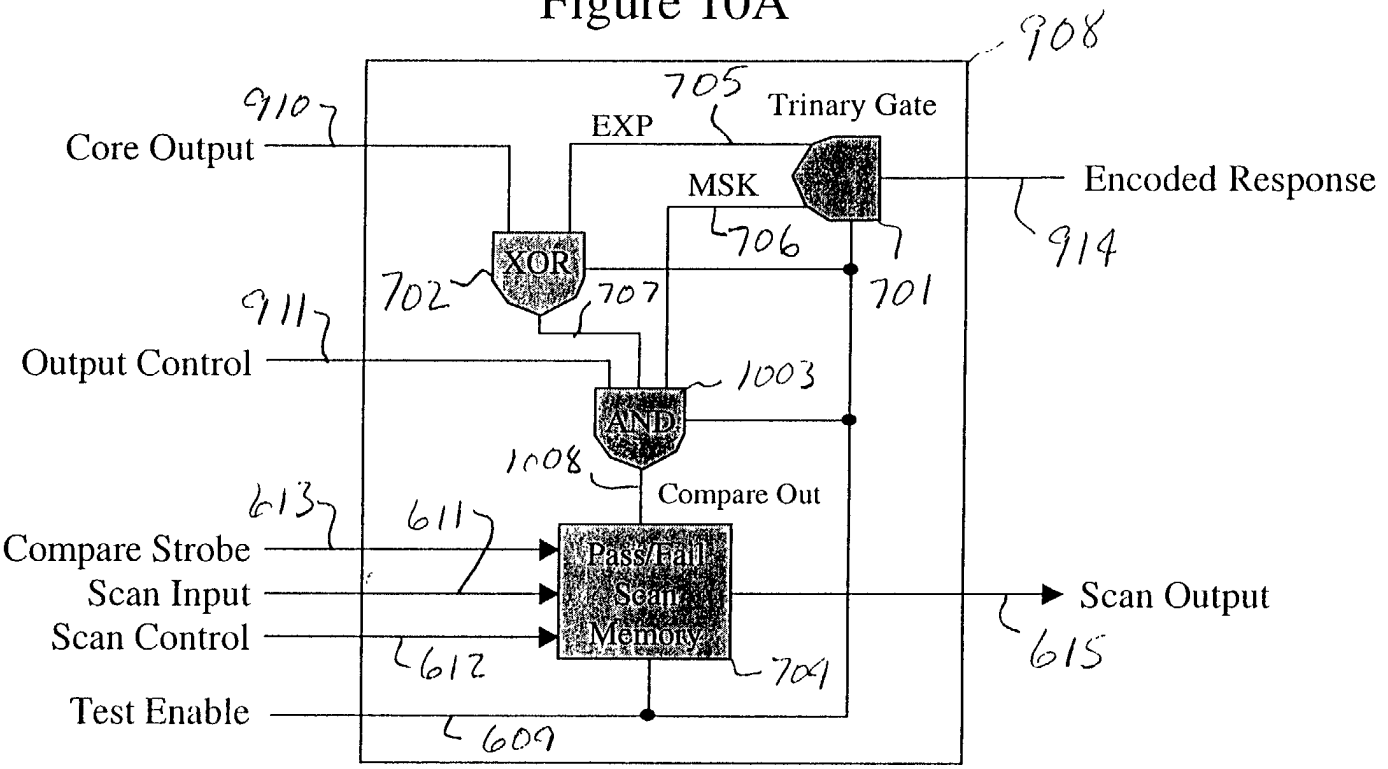


Figure 10B

OC	TEN	ENR	MSK	EXP	Function Performed
X	0	X	X	X	Test Disabled
1	1	Gnd	1	0	Compare Low
1	1	Vdd	1	1	Compare High
1	1	1/2Vdd	0	X	Mask Compare
0	1	Gnd/Vdd	1	0/1	Test Output Control

Adapting Die Input/Outputs
To Support Improved Wafer Testing

Figure 11A

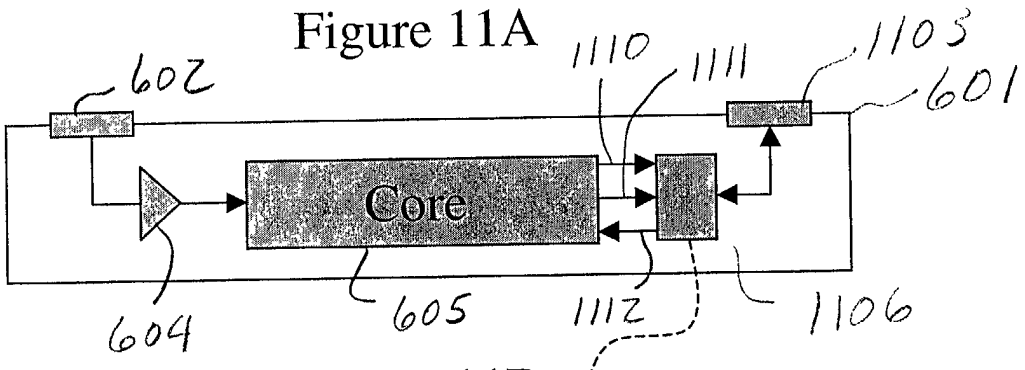
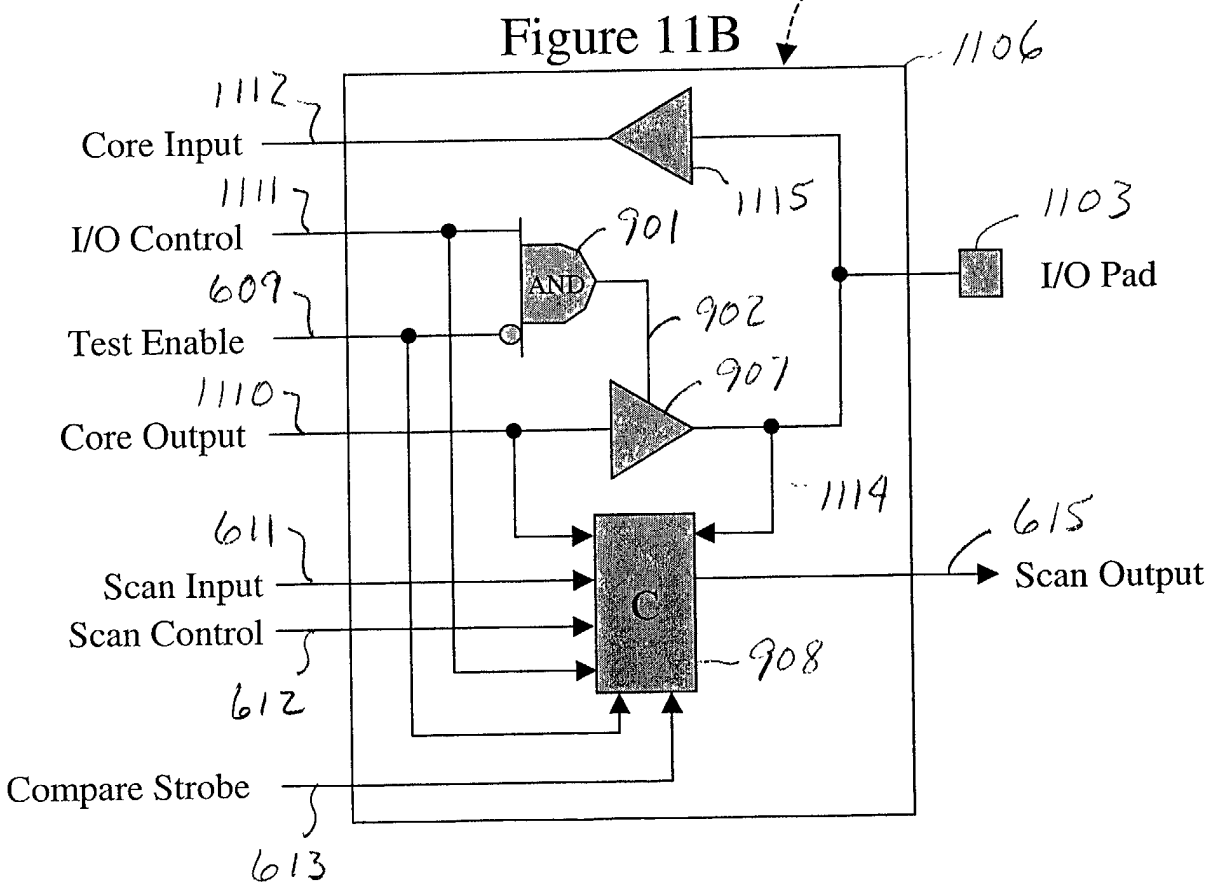


Figure 11B



Maskable Comparator For Input/Outputs

Figure 12A

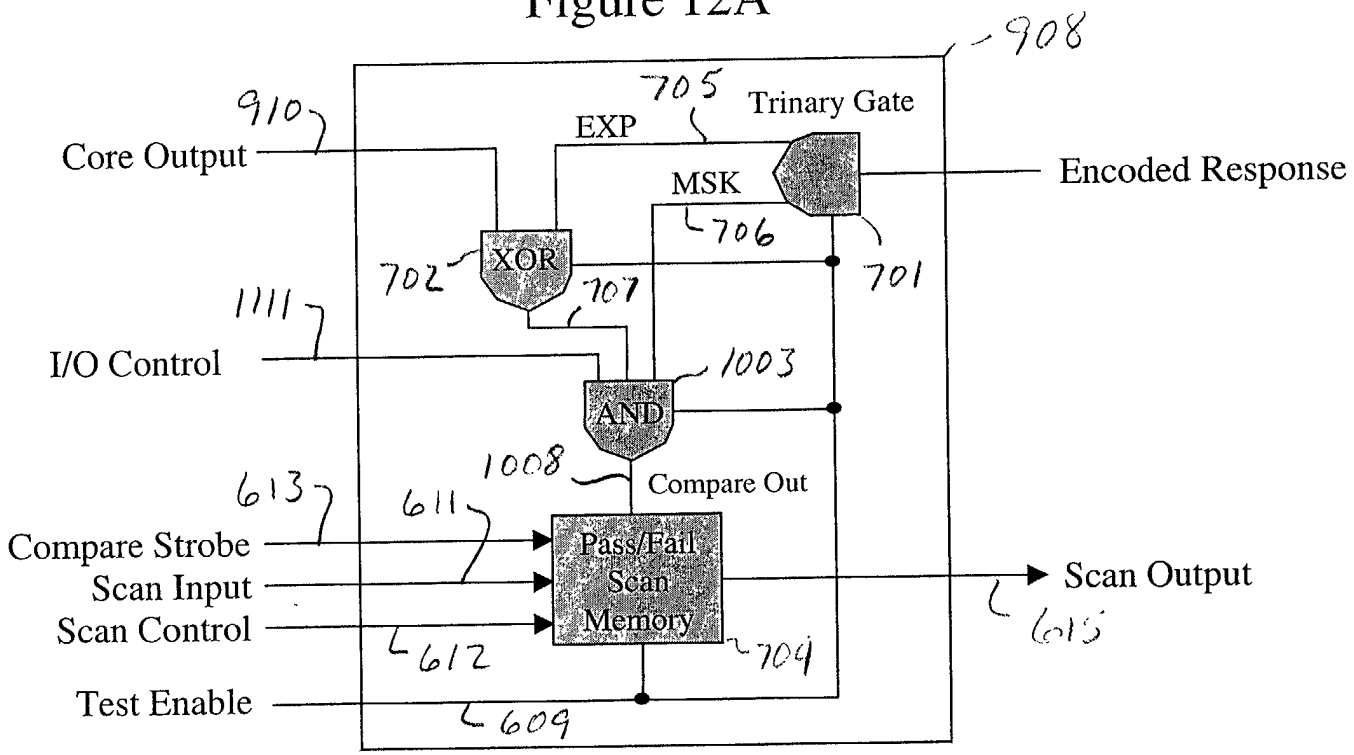


Figure 12B

IOC	TEN	ENR	MSK	EXP	Function Performed
X	0	X	X	X	Test Disabled
1	1	Gnd	1	0	Compare Low
1	1	Vdd	1	1	Compare High
1	1	1/2Vdd	0	X	Mask Compare
0	1	Gnd/Vdd	1	0/1	Test I/O Control
0	1	Gnd/Vdd	1	0/1	Input Stimulus

Fail Output for Diagnostic Testing

Figure 13A

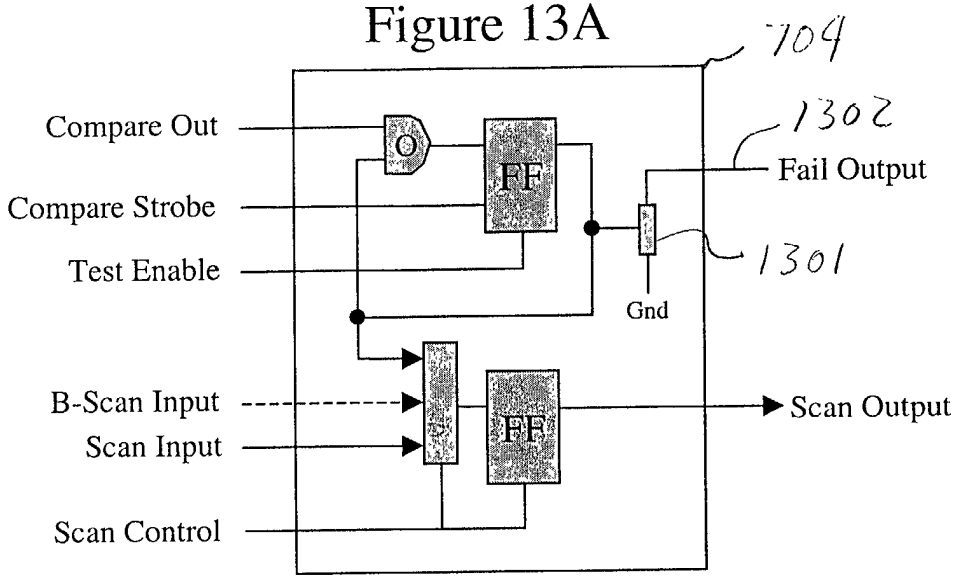
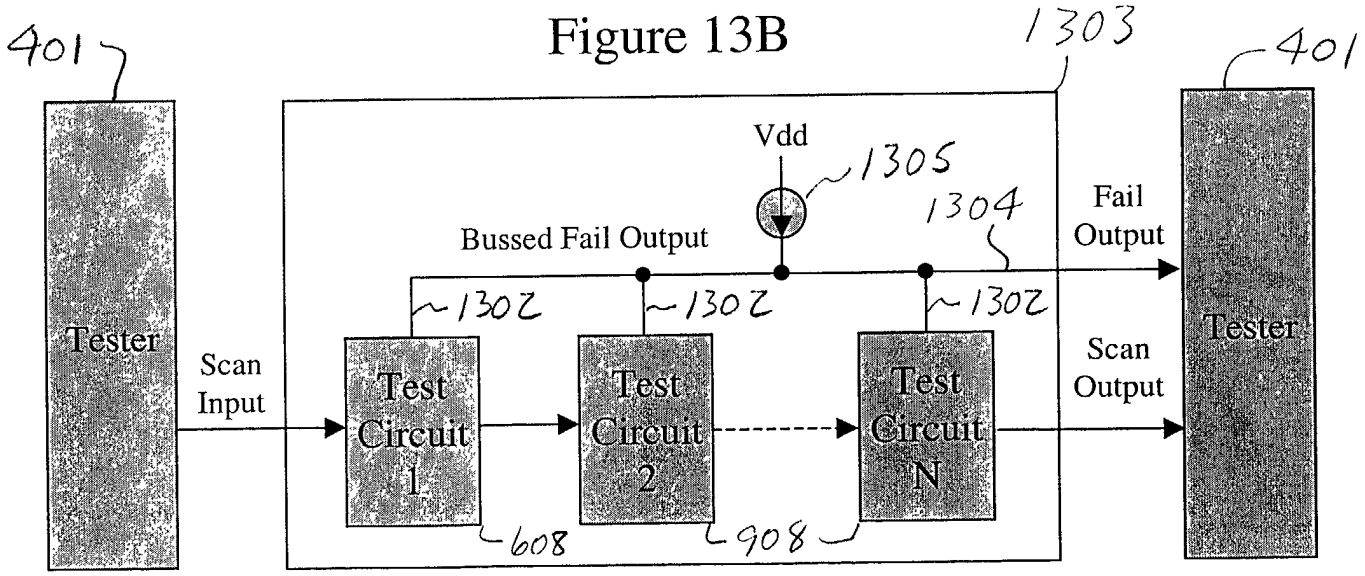
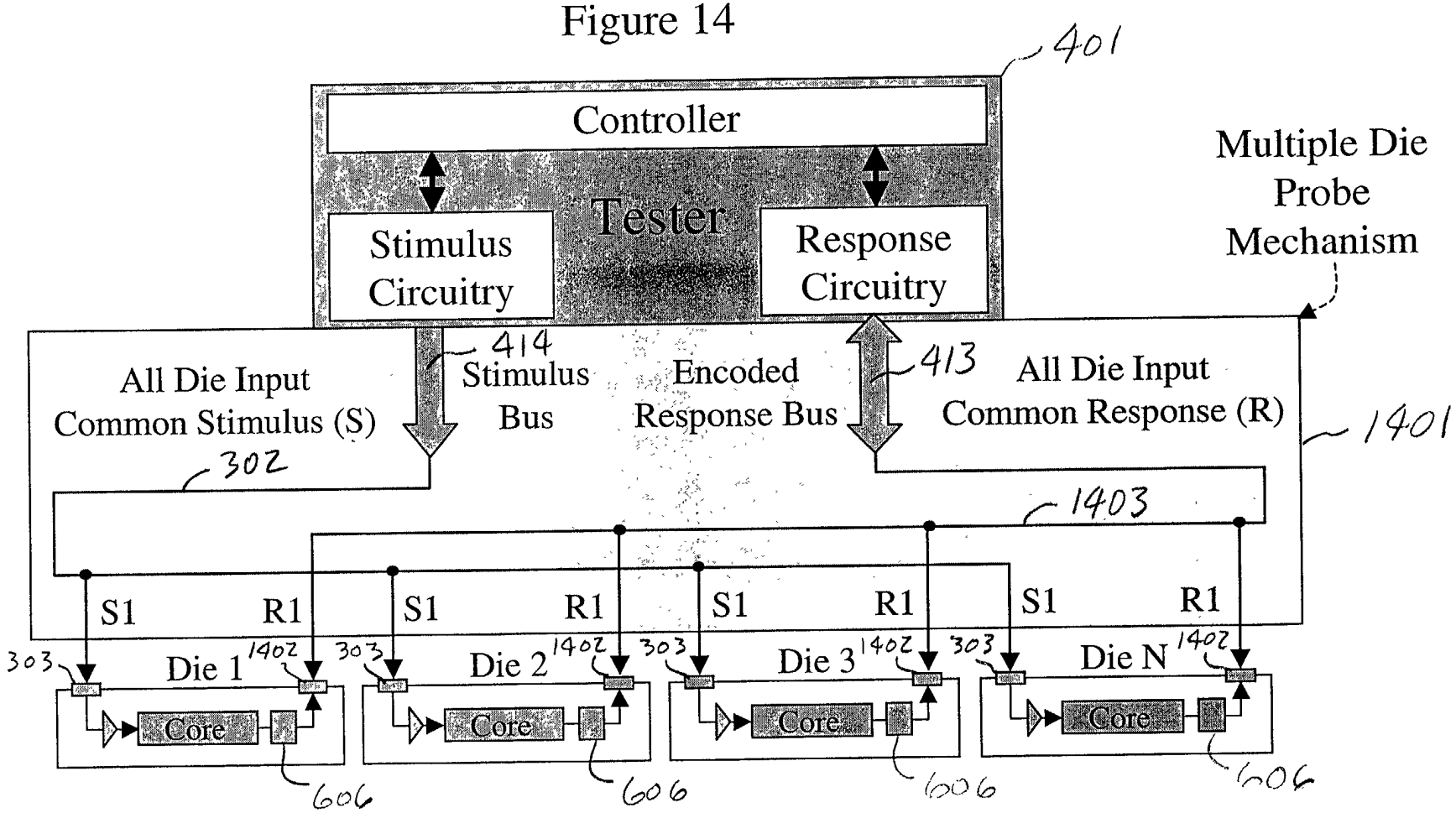


Figure 13B



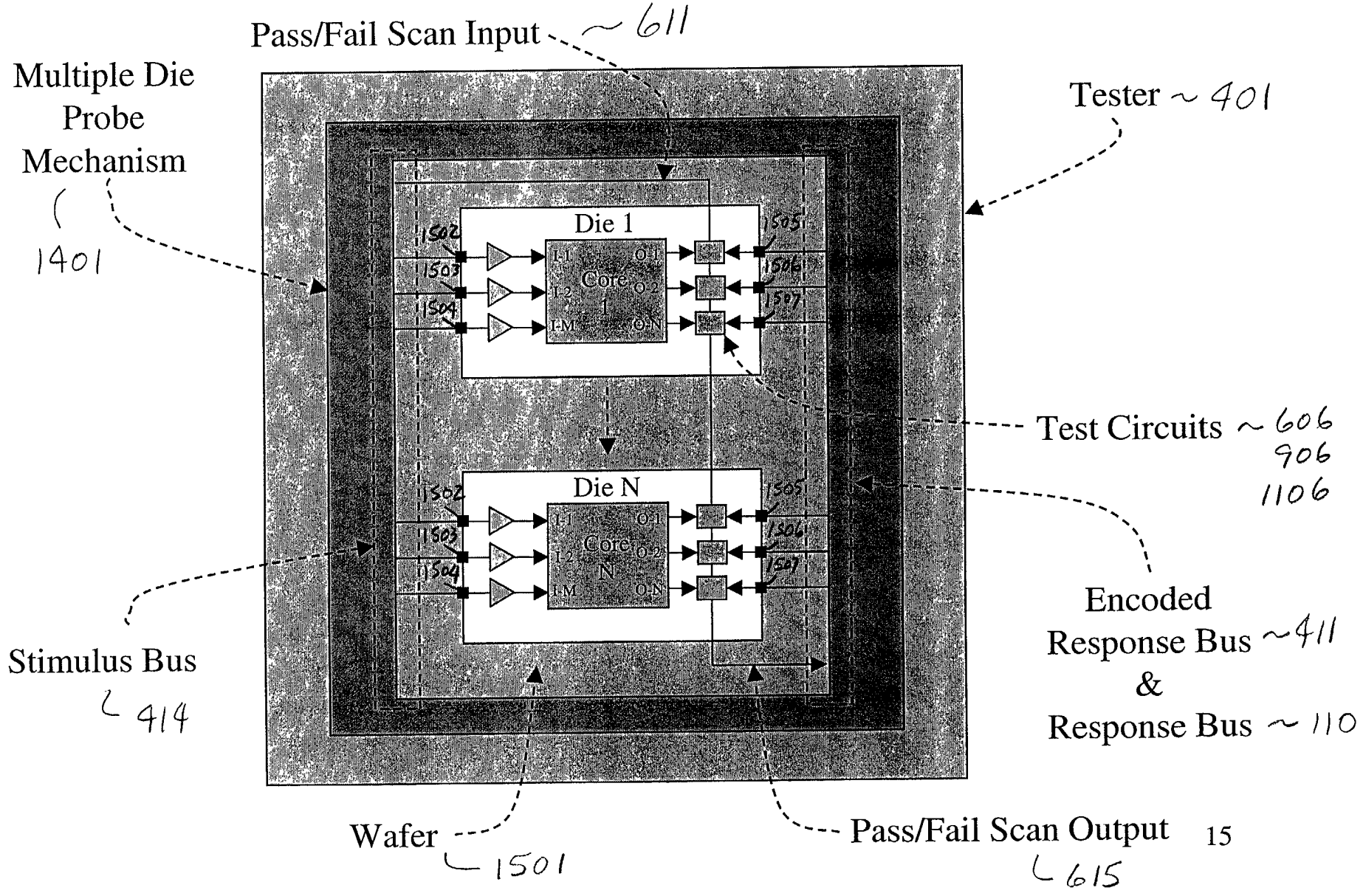
Improved Multiple Die Probe Test Example

Figure 14



Conceptual View of Improved Die Test

Figure 15



Die Being Tested in Functional Mode

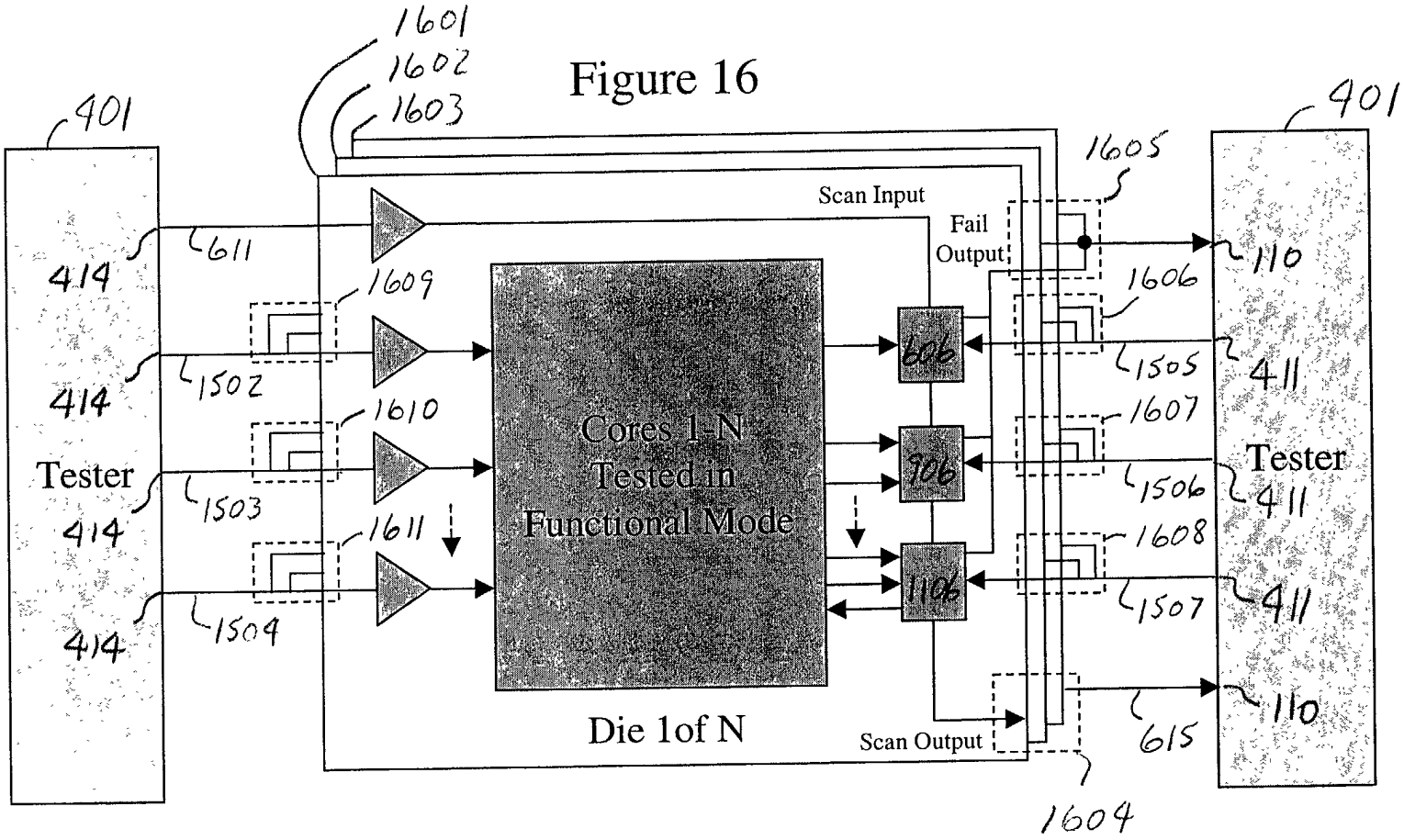


Figure 16

Die Being Tested in Scan Mode

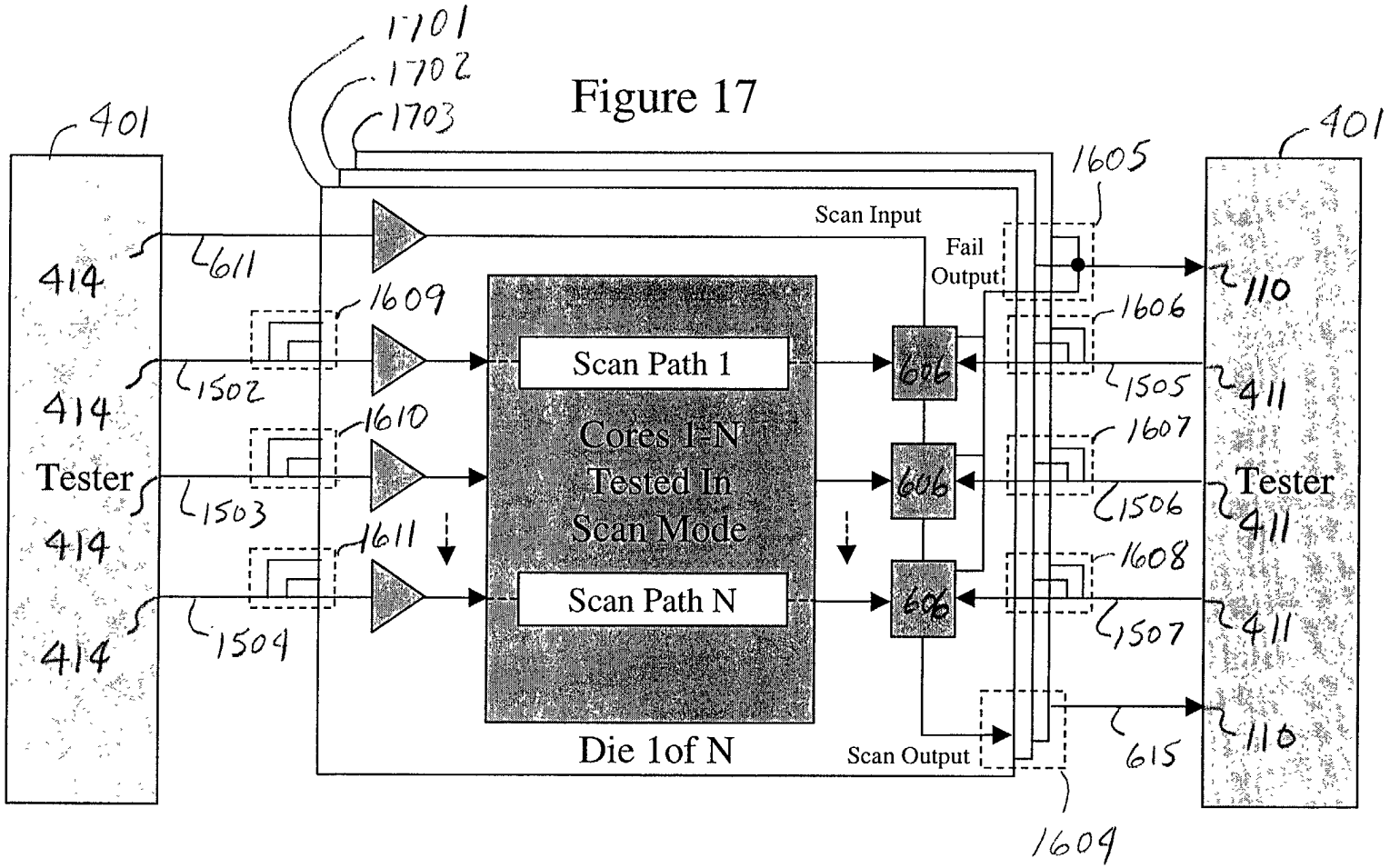


Figure 17

Testing System-On-Chip Die having
Multiple Embedded IP Core Sub-Circuits

Figure 18A

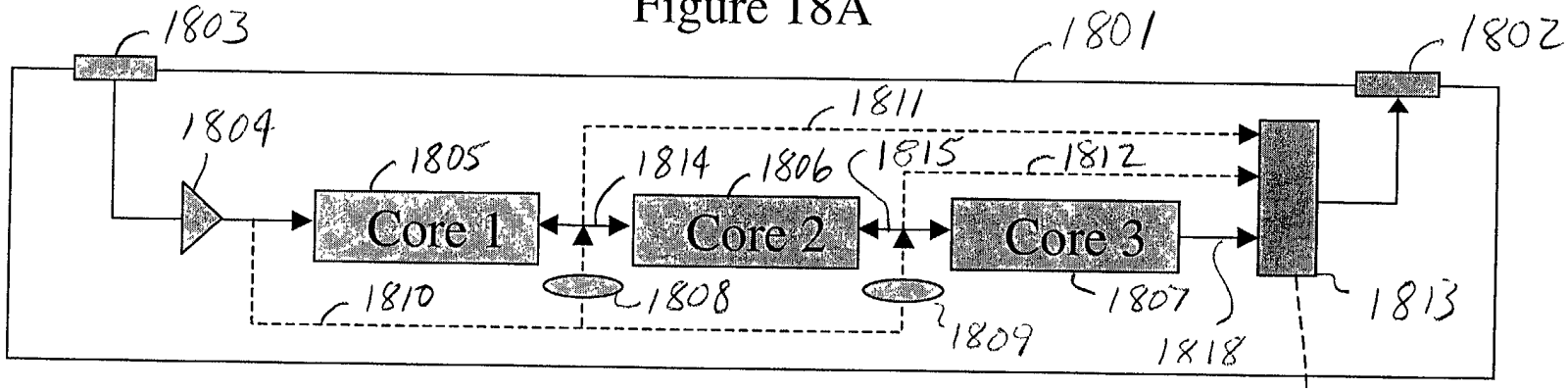
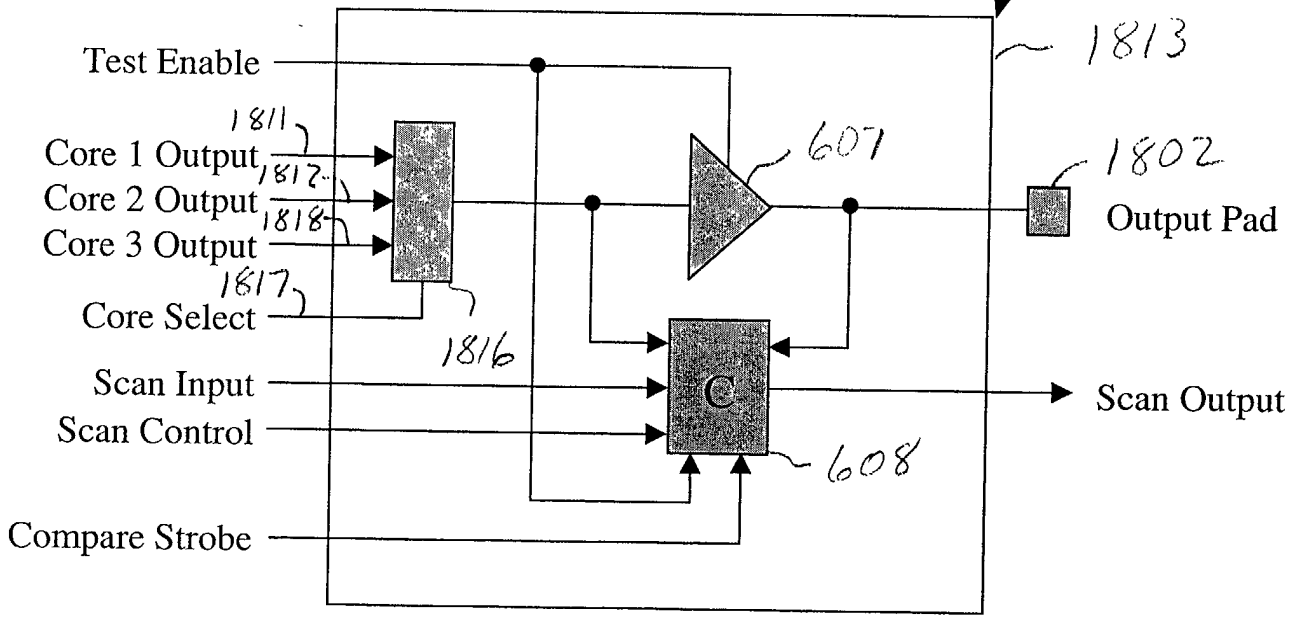
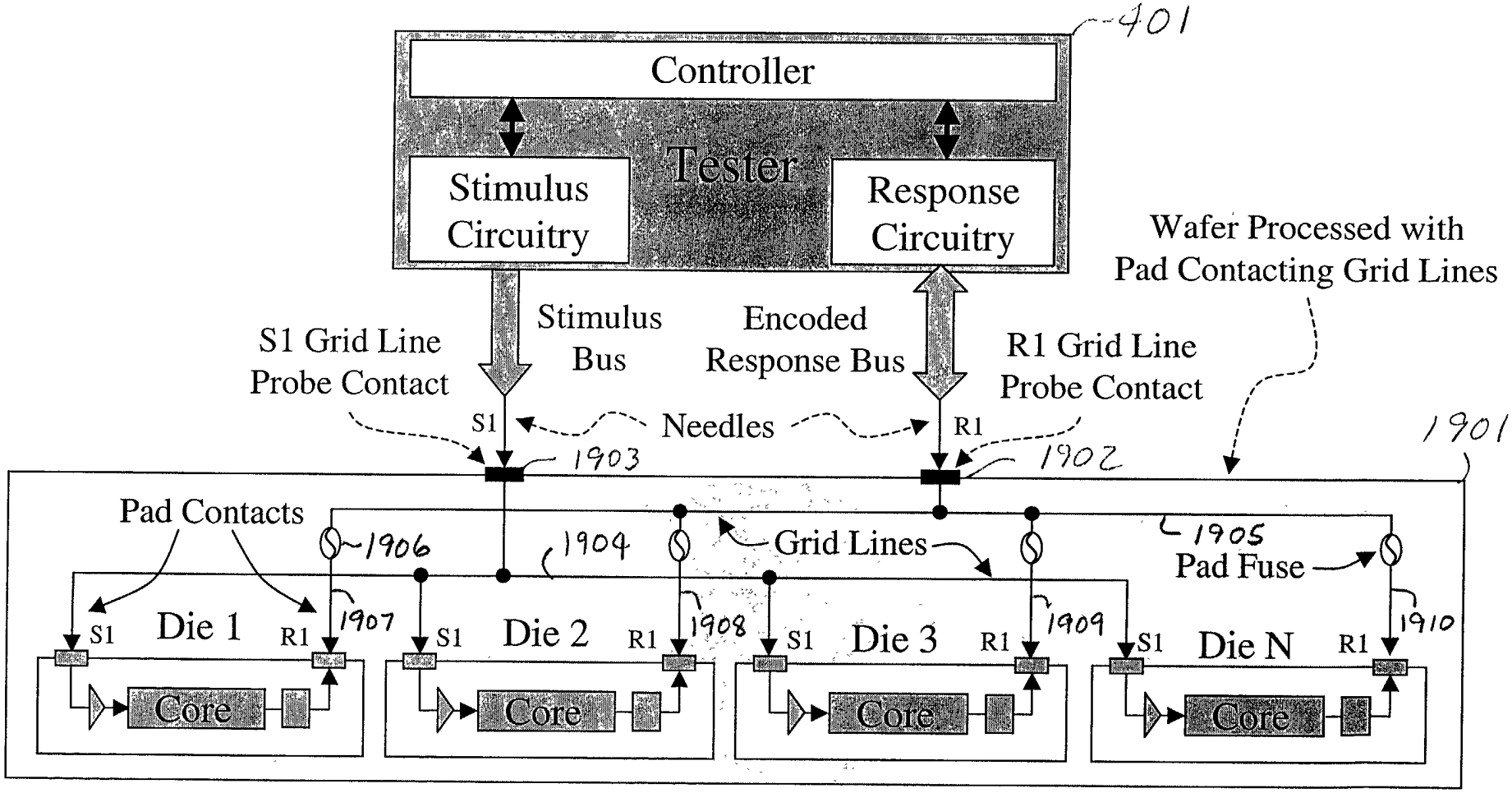


Figure 18B



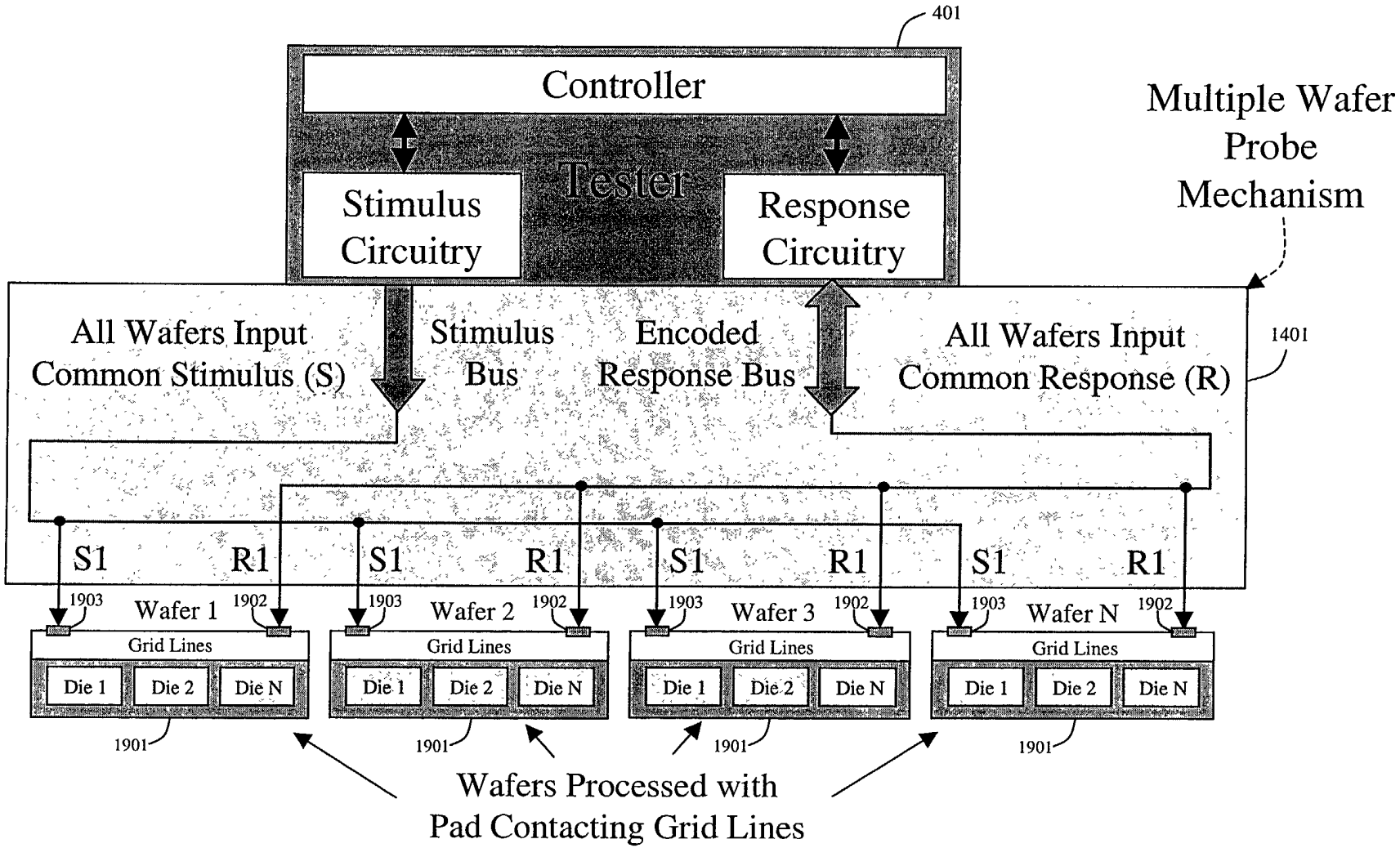
Adapting Wafers
To Support Improved Wafer Testing

Figure 19



Improved Multiple Wafer Test Example

Figure 19A



Improved Multiple IC Test Example

Figure 20